INCREASING DIGITAL DATA SENT WITH PULSE CODE MODULATION METHOD
(PENINGKATAN PENGIRIMAN DATA DIGITAL DENGAN METODE PULSE CODE MODULATION)

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ABSTRACT

The telemetry data of the sounding rocket when flying in the space is very important to known. This data will be used for next mission or evaluation the last rocket flight. Commonly the data of the sensor in the sounding rocket are accelerometer, gyroscope, magnetometer, GPS. The rocket is required to transmit maximum data to the ground control system when it flies. The problem is when the baud rate is low, there is not much data can be transmitted. Another problem is when using serial bit standard communication such as the baud rate 115200 bps means that the maximum data in one second is 14,400 characters. It is less than when using the PCM bit rate. Application of PCM in the telemetry for sounding rocket LAPAN is new and needs further development to reach the optimal function. The communication data can transmit around 1.25Mbps or 156,250 characters based on the TR FM02-S-2 full S-band transmitter by using PCM method. This research focuses the implementation of PCM method on the FPGA for sending and receiving the data via cable. Two FPGA boards can work together for sending and receiving the data using PCM method with the total bit is 1.25Mbps.

Keywords***:*** *PCM, FPGA, BCD*

ABSTRAK

Pengiriman data dari roket sonda ketika terbang adalah sangat penting untuk diketahui. Data tersebut akan digunakan sebagai bahan evaluasi dari hasil uji terbang atau misi uji terbang berikutnya. Secara umum sensor pada roket sonda terdiri dari accelerometer, gyroscope, magnetometer dan GPS. Sebuah telemetri roket memerlukan pengiriman data ke pusat penerima sebanyak-banyak ketika terbang. Permasalahan akan timbul jika kecapatan pengiriman data pada per detik sangat rendah, sehingga tidak banyak data yang bisa dikirimkan. Persoalan lainnya adalah kecepatan pengiriman data dengan standar serial yaitu 115.200 bit atau 14.400 karakter per detik, hal ini masih rendah jika dibandingkan dengan menggunakan metode PCM. Penggunakan metode PCM di pusat teknologi roket merupakan hal baru sehingga diperlukan pengembangan untuk mencapai fungsinya secara optimal. Dengan menggunakan metode komunikasi PCM maka data yang dapat dikirmkan bisa mencapai 1,25 juta bit atau 156.250 karakter per detik berdasarkan spesifikasi dari radio TR FM02-S-2 dengan frekuensi S-band. Penelitian ini fokus pada penerapan metode PCM dengan menggunakan modul FPGA sebagai pengirim dan penerima dengan menggunakan kabel sebagai media transmisi datanya. Dari hasil pengujian diperoleh bahwa dua modul FPGA tersebut dapat berfungsi sebagai pengirim dan penerima data dengan metode PCM sampai dengan kecepatan 1,25 juta bit per detik.

Kata kunci ***:*** *PCM, FPGA, BCD*

1 Introduction

The Rocket technology center (Pustekroket) LAPAN is the government institution for sounding rocket research in Indonesia. The development of sounding rocket to bring the weather station payload or satellite into the orbit in the future. There are many types of sounding rocket have been developed by Pustekroket such as; RKX-100 (rocket control experiment, RTX-100 (rocket tail experiment), RWX-200 (rocket wing experiment) (Kurdianto, 2015). All of onboard computer for those rocket types are typically the same which consisted of accelerometer sensor, gyroscope sensor, magneto sensor, and GPS (global positioning system) and the microcontroller ATMEGA 32 8 bits processor. The combination of those sensors are known as inertial measurement unit (IMU) to measure the attitude of the rocket when flying (Mudarris, 2020).

The important thing in the development of the sounding rocket is how to send the rocket's data from the transmitter on the rocket and receiver on the ground control system (GCS). High-rate telemetry data is very important on the rocket technology (Zhu, 2016). Transmitting the data of rocket's sensor needs the radio transceiver which has the same frequency and speed of sending bit data. Until now the radio transceiver maxstream 900 MHz is always used in the telemetry of Sounding rocket in Pustekroket. Due to the communication data between sub systems in the onboard computer is used the serial TTL with the baud rate 115200 bps, so the radio transceiver also used that baud rate. With that baud rate speed, the maximum character on one second can transmitted data 14,400 characters. In the flight test of the sounding rocket, maximum possible data must be sent to the GCS, since knowing the attitude of the rocket become very important.

Aerospace standard communication or telemetry data doesn’t use the serial TTL for communication each other components or equipments. The standard communication uses IRIG106 with the format pulse code modulation. From 2019, Pustekroket telemetry department started the research on the pulse code modulation to increase the telemetry data for sounding rocket. Pustekroket has the mobile GCS from zodiac French with telemetry data based on PCM. Figure 1-1 is the zodiac mobile ground control system. This system is connected with radio transmitter TR FM02-S-2 with speed data of PCM format is 1.25 Mbps. Figure 1-2 is radio transmitter TR FM02-S-2 with frequency working is 2.4 GHz.

Figure 1-1 : Zodiac Ground Control System Mobile

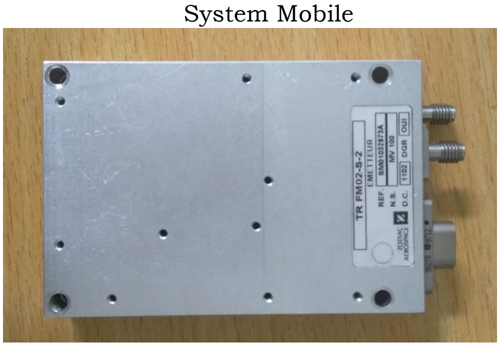

Figure 1-2 : Radio TR FM02-S-2

The methodology in this research is using two boards FPGA cyclone V for communication each other with using PCM format. One board FPGA for reading the sensor and convert it to PCM format or as modulator. The other FPGA board for receiving the data, and then do demodulation as modulator after the data is sent to the computer via serial TTL. The communication between 2 FPGA boards are directly using 2 wires, one wire as data and the other wire as ground. For programming, the FPGA Cyclone V uses free Quartus II type and programming language is VHDL (very high speed hardware description language).

This paper focuses on the pulse code modulation method to increase the digital data sent . In the future research, this method will be implemented on the radio PCM TR FM02-S-2 as shown in the Figure 1-2.

2 Theoritical Background and Methodology

Pulse code modulation has two functions, the first function is for converting analog signal to digital signal (Rahman, 2014), and the second is for telemetry data format (Sudjendro, 2017). Pulse code modulation system can be used to increase the telemetry data (Zhu, 2016). PCM communication can be simulated with a software virtual such as LabView before implemented to the hardware (Rahman, 2014). Another study in (Gupta, 2016) uses simulink to transmit analog signal for PCM performance. In the PCM process there are several step; sampling, quantization, and encoding. PCM method also can be converted as circuit of digital pulse position modulation (Bhat, 2009).

Sampling is the process to take the signal input with a certain time or frequency, due to some of the input is more than one. According to the Nyquist theory, the frequency of the sampler is minimum 2 times of the frequency of the input signal (Lévesque, 2014). The nyquist sampling rate is B < $f_s/2$ where B is bandlimit and fs is frequency sampling. The sampling signal input result will be quantized to get the value. The last process is coded the quantized value to become digital signal with level 1 and zero. The level 1 represents 5 volt and the 0 represents 0 volt.

According (Gupta, 2016) that PCM has advantage and disadvantages in application. The advantages of PCM are; reduce of noise effect, PCM can support pulse regeneration, possibility of multiplexing for various PCM signals, for transmitting signal can be placed the repeater due to the PCM signal is digital. These following are some of disadvantages from PCM; the process on PCM is complex which including sampling-quantization-encoding, it also needs huge bandwidth on the processing transfer data.

The methodology of this research is converting the ADC value become PCM signal by FPGA encoder and then that signal transmitted to another FPGA decoder. Therefore, the process sampling and quantization are conducted by ADC on the DE0-Nanos-Soc board. The FPGA decoder will read the PCM signal and then send it to the computer. According the packet data as shown in Figure 2-1 which is PCM format for zodiac system, thus the input analog signal of ADC is small part of the full packet PCM format. The diagram line of the system this PCM methodology is shown in Figure 2-2a. According diagram line that change the analog signal become PCM signal by FPGA.

Figure 2-2b is the flow chart of the encoder from ADC data digital signal to the PCM format. Each line data must have header to indicate that is the first column of the data in one line. Figure 2-2c is decoder of PCM signal which has task to interpret the PCM signal and then convert it to BCD format. BCD data will be sent to computer via TTL serial to USB converter and then displayed it to GUI as shown in Figure 4-6.

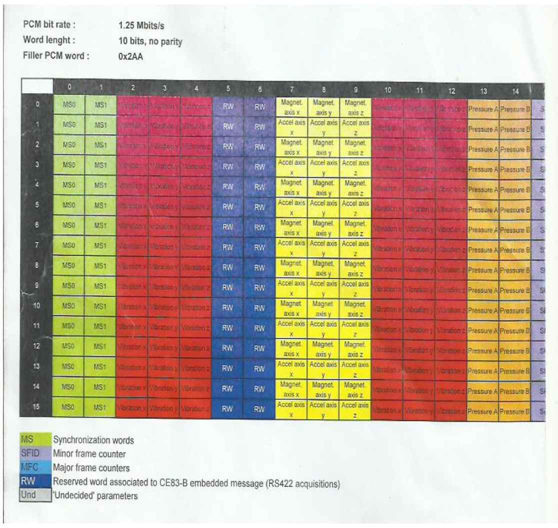

Figure 2-1 : PCM Data Structure

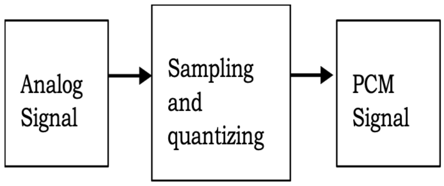

Figure 2-2a : Diagram Line PCM

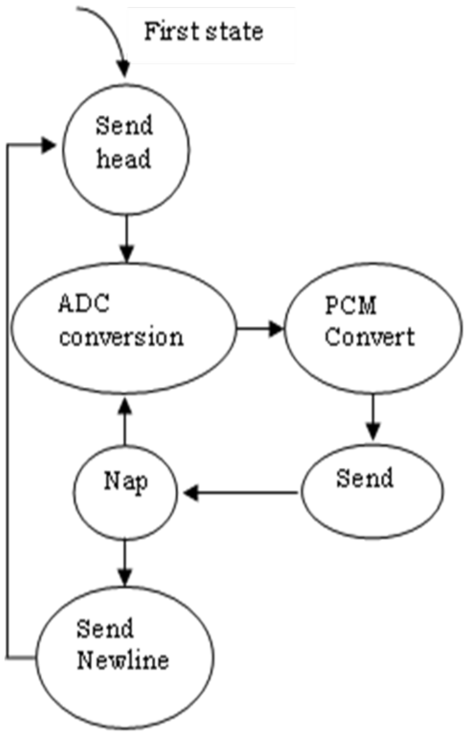

Figure 2-2b : Flow Chart of Encoder

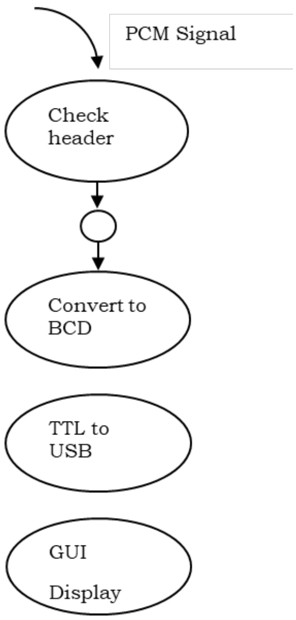

Figure 2-2c : Decoder Flow Chart

3 FPGA Platform Module

The module FPGA DE0-Nano-Soc was chosen to realize the main functions of the system interface PCM format a, because it is easy to operate. The module contains an Altera Cyclone V 5CSEMA4U23C6N FPGA, some electronic components, LED, buttons, and a USB JTAG for interfacing to a PC. The module is simply plugged into the computer thus quick start of developed VHDL programming. A module FPGA DE0-Nano-Soc is shown in Figure 3-1 and its property is given in Table 1 (Field, 2018). The Altera Cyclone V contains two systems; FPGA (field programmable gate array) and HPS (hard processor system). Processing PCM is done by FPGA.

Figure 3-1 : FPGA Board (Terasic.com, 2020)

Table 3-1: Property of DE0-Nano-Soc

DE0-Nano-Soc Board	
FPGA	HPS
Altera Cyclone V SE 5CSEMA4U23C6N	925MHz Dual-core ARM Cortex-A9 processor
Serial configuration device-EPCS128	1 GB DDR3 SDRAM
USB-Blaster II	1 Gigabit Ethernet
2 push-buttons	Port USB OTG
50 MHz clock sources	Micro SD card socket

The FPGA ICs are usually designed using hardware description languages (HDLs) such as verilog or VHDL in Quartus II IDE environment. Before the VHDL coding deployed to the FPGA, it can be simulated with the software ModelSim. From this simulation it can be known the input and output logic of application.

4 Experimental Result

The proposed diagram circuit has been implemented in the interface between two boards FPGA and FPGA board receiver to the computer for performance evaluation. The setup experiment is shown in the Figure 4-1. The first FPGA board as the encoder PCM and the second FPGA board as the decoder PCM. The first FPGA board read the analog input and then change it becomes the PCM data. The second FPGA board will decodes PCM data from the first board and then transmits it to the computer via TTL serial to USB. Furthermore, the clock signals from the FPGA board decoder as well as the FPGA board decoder were assumed synchronous with each other. The results of experimental investigation conducted based on the proposed scheme are shown in the Figure 4-1 to Figure 4-5. The output PCM signal and the synchronous pulse are shown in

Figure 4-3. The yellow pulse is the synchronous pulse with 4.18 ms or 240.385 Hz. Blue signal on the oscilloscope is PCM signal or data.

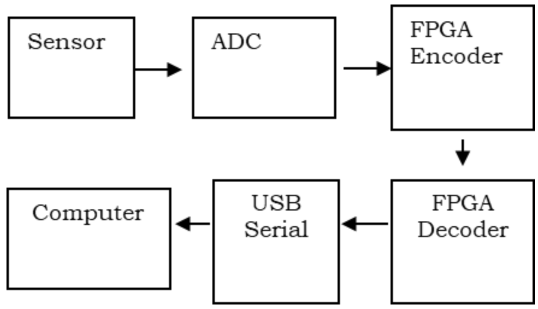

Figure 4-1 : Setup Experiment

Implementation of VHDL program onto FPGA board for reading ADC can be simulated with ISim simulator. Figure 4-2 is the simulation results of reading ADC depends on the design.

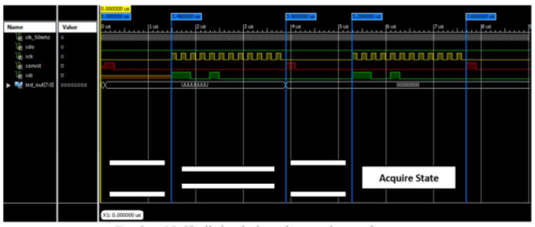

Figure 4-2: Simulation Result of Reading ADC

The output of the ADC is binary12 bit, before this data is sent to the computer, it must be converted to BCD with 16 bits. Each four bits in BCD represents number thousand, hundreds, dozens, unit. Conversion BCD to ASCII value must be add value 3 or binary 0011. The conversion process from binary to BCD in FPGA algorithm is conducted according Figure 4-5. Figure 4-4 is the data which is sent to the computer via serial to USB. Figure 4-6 is GUI for displaying the PCM data with the interface control. It is one by one display graph or together.

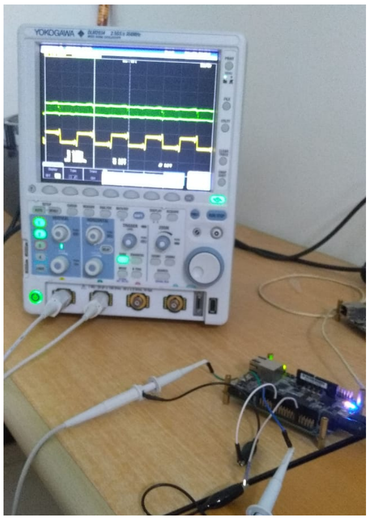

Figure 4-3: Checking Pulse PCM with Oscilloscope

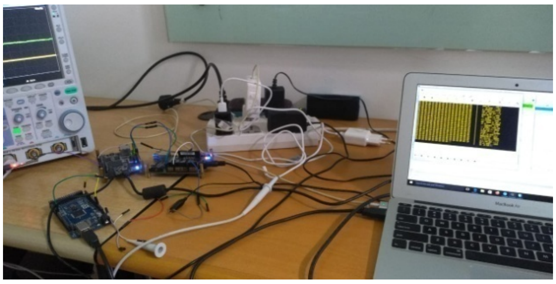

Figure 4-4: Sending PCM data to Computer

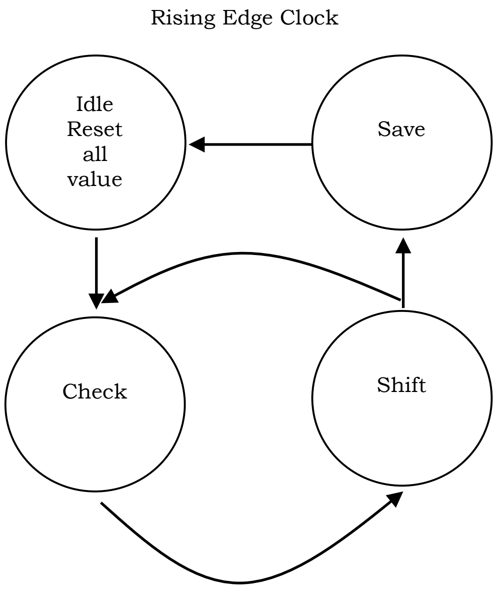

Figure 4- ary
to BCD

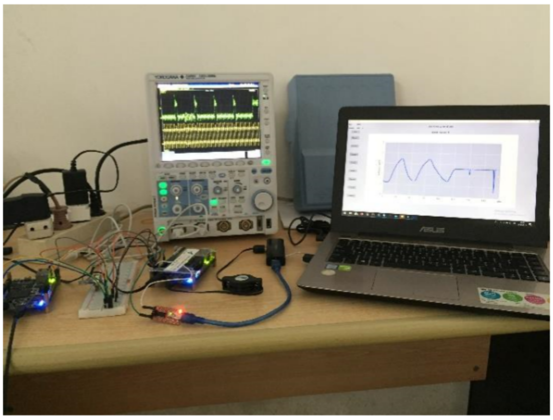

Figure 4-6: GUI Display of Result PCM data

According to the Figure 1-2, the format data of radio TMRF PCM is 1.25 Mbps/s. Thus 1.25 million bits can be transmitted to the radio in 1 second. One bit has the time 0.8 uS as shown in Eq. (4-1). Board FPGA DE0-Nano-Soc has clock with frequency 50MHz, thus the time for one pulse is 0.02 uS as calculated in Eq. (4-2). According to the clock time, the FPGA can handle to make a pulse with time 0,8 us.

$$t_{bit} = \frac{1s}{1,250,000} = \frac{1,000,000\ \mu s}{1,250,000} = 0.8\ \mu s \quad (4\text{-}1)$$

$$t_{clk} = 1/50\text{MHz} = \frac{1,000,000}{50,000,000\ Hz} = 0.02\ \mu s \quad (4\text{-}2)$$

5 Conclusion and Future Work

Reading analog input and then converts it to the PCM signal has been conducted by the first FPGA board as the transmitter. The first FPGA board transmits the PCM signal to the second FPGA board with 2 wires, 1 wire as the PCM signal line and another wire as the synchronized signal. The PCM data is displayed by computer after receiving the data from the second FPGA board.

The next working is integrating the first FPGA board to the radio PCM TR FM02-S-2 as transmitter. Monitoring the data will use the ground mobile system zodiac which is compatible with radio PCM TR FM02-S-2.

Acknowledgment

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